WIRED E-RL LOCK

DATA SHEET

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AXA Stenman
EnergieStraat 2
3903 AV Veenendaal
Netherlands
http://www.axa-stenman.com/
T: +31 318 536 111
F: +31 318 595 535
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Table of Contents

1. INTRODUCTION 5

2. PHYSICAL INTERFACE 6

MICROCONTROLLER MODE 7
H-BRIDGE CONTROLLED MODE 7
H-BRIDGE POWERED MODE 8
SWITCHES CONTROLLED MODE 8

3. OPERATION 9

UNLOCKED MODE – SECURED / UNSECURED / UNEXPECTED 9
MICROCONTROLLER MODE – POWER UP 10
MICROCONTROLLER MODE – UNLOCKING / LOCKING 11
H-BRIDGE CONTROLLED MODE – POWER UP 13
H-BRIDGE CONTROLLED MODE – UNLOCKING / LOCKING 14
H-BRIDGE POWERED MODE – POWER UP 17
H-BRIDGE POWERED MODE – UNLOCKING / LOCKING 18

4. DESIGN CONSIDERATIONS AND RECOMMENDATIONS 21

5. TEST SCENARIOS 21

6. ELECTRICAL CHARACTERISTICS 22

APPENDIX A – TEST SCENARIOS 23

1. Introduction

The highly flexible wired eRL lock can be controlled and interfaced directly through microcontroller I/O pins without the need for any additional control interfacing, like level converters, buffers or high power drivers. However it is also possible to directly control and interface the eRL through a standard H-Bridge configuration, replacing a simple dc-motor or solenoid controlled lock. It is even possible to control the eRL using simple momentary switches without any additional hardware, all debouching of the control interface is handled inside the eRL. The wide voltage operating range combined with the flexible interface makes it easy to integrate the eRL into existing or new designs.

The microcontroller based eRL takes all complicated lock handling and timing out of the hands of the user and offers a simple straightforward interface to power, control and monitor the eRL. The lock also employs an extreme low power saving mode minimizing current consumption to maximize battery life while offering fast response to control commands.

2. Physical interface

The connector used is the Molex SPOX Header 22-03-5055 or Molex C-Grid Header 90120-0125, pin layout and function description is given in the table below.

Pin layout:

1. Power Vdd (Typ. +8V)
2. Logic Input: A
3. Power Vss (Gnd. 0V)
4. Logic Input: B
5. Logic Output: Status (Open drain output)

Status Output (Pin 5)	
Lock Open	Low
Lock Closed	Floating

The interface is using a total of 5 wires for maximum flexibility, two wires are used as power lines. Maximum voltage and current ratings are given in Chapter 6.

Command input	**A (Pin 2)**	**B (Pin 4)**
Lock Idle	Low	Low
Lock Idle	Floating or High	Floating or High
Lock Opening	Low	Low -> High
Lock Opening	High -> Low	High
Lock Opening	High -> Low	Low -> High
Lock Closing	High	High -> Low
Lock Closing	Low -> High	Low
Lock Closing	Low -> High	High -> Low

The remaining wires are used to control the operation and read the status of the eRL. Logic inputs A and B are used to control the opening and closing of the eRL while the logic status output (open drain output) is used to read the current lock state. The picture in Figure 1 is showing clearly the location of pin 1.

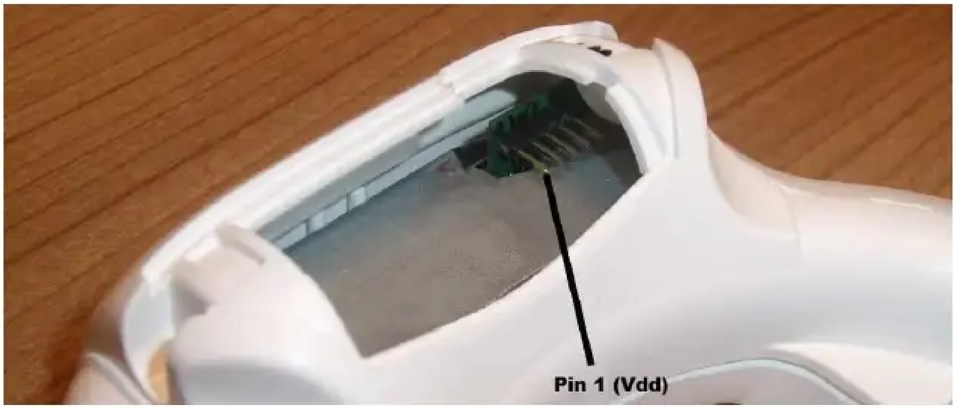


Figure 1.

Microcontroller Mode

The eRL lock can be controlled and interfaced directly through microcontroller I/O pins without the need for any additional control interfacing, like level converters, buffers or high power drivers. Figure 2 is giving a standard interface solution for 3.3V and 5V microcontrollers. The Pull-Up resistor needed for the open-drain status output can be either internally or externally to the microcontroller.

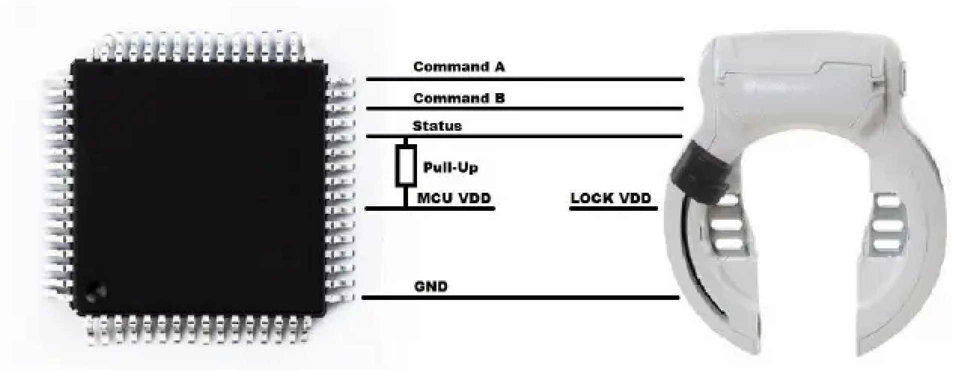


Figure 2.

H-Bridge Controlled Mode

The eRL lock can be controlled and interfaced directly through a standard H-Bridge configuration, replacing a simple dc-motor or solenoid controlled lock. Figure 3 is giving a standard interface solution for H-Bridges. The open-drain status output is available for lock status feedback, a Pull-Up resistor internally or externally to the microcontroller is needed for proper operation.

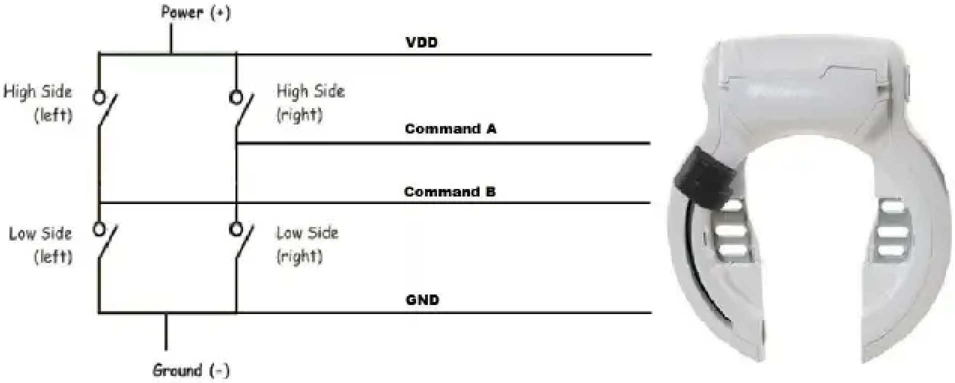


Figure 3.

H-Bridge Powered Mode

The eRL lock can be powered, controlled and interfaced directly through a standard H-Bridge configuration, replacing a simple dc-motor or solenoid controlled lock. Figure 4 is giving a standard interface solution for H-Bridges. The open-drain status output is available for lock status feedback, a Pull-Up resistor internally or externally to the microcontroller is needed for proper operation.

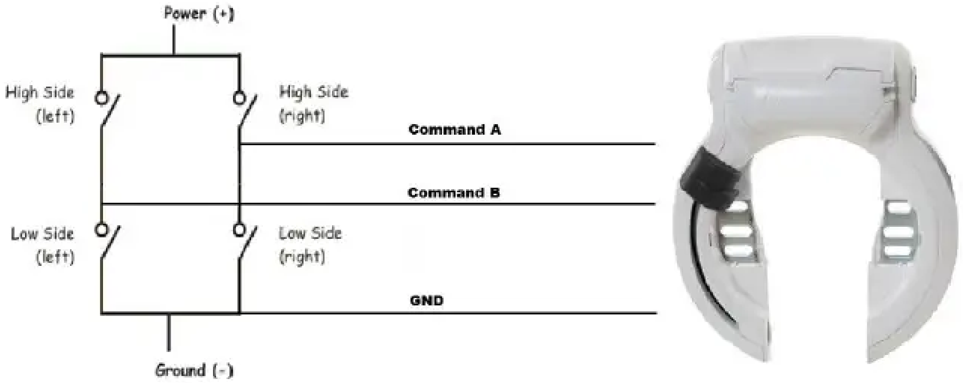


Figure 4.

Switches Controlled Mode

The eRL lock can be controlled and interfaced directly using two simple momentary switches without any additional hardware, all debouching of the control interface is handled inside the eRL. The green LED in series with the 3K3 resistor is reporting when the lock is open. The schematic for the switches controlled eRL lock is given in Figure 5.

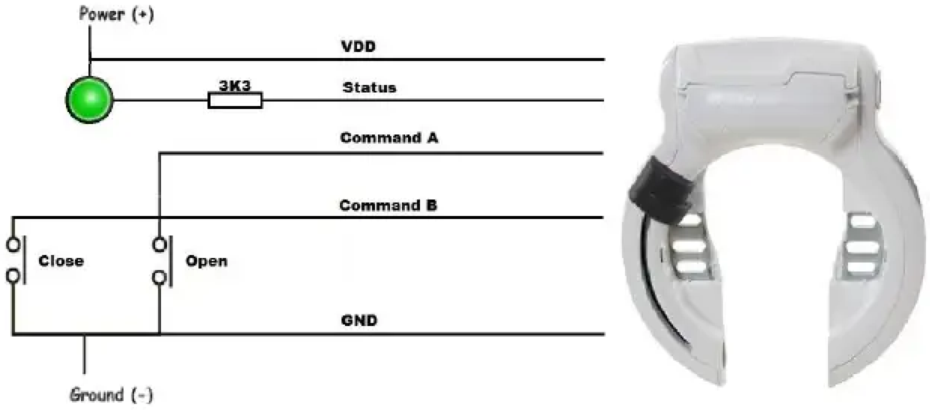


Figure 5.

3. Operation

The operation and control of the eRL is done through two ports, logic input A and B are used to open and close the lock while the logic status output port is giving the current lock state. While the eRL is powered but not operated the unit will go automatically into an extreme low power saving mode reducing current consumption to the absolute minimum. This extreme low power saving mode makes it possible to leave the lock powered at all times without wasting valuable energy and still responding fast to user commands and able to read the lock status instantly compared to a power-down/power-up/power-down scenario. The power-down to power-up sequence takes 500ms initialization time before the lock can be operated or valid lock status information is provided. We therefor advice to always power the eRL lock even if it’s operated infrequently.

Unlocked Mode – Secured / Unsecured / Unexpected

Figure 6 presents the condition the leaver is in when the lock is Unlocked and the leaver is secured. This is the normal condition the lock is in when Unlocked.

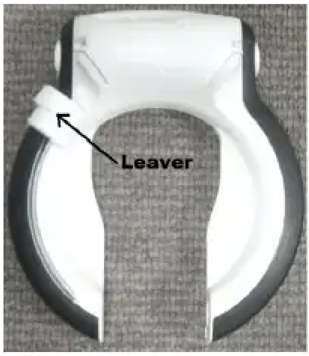


Figure 6. – Unlocked

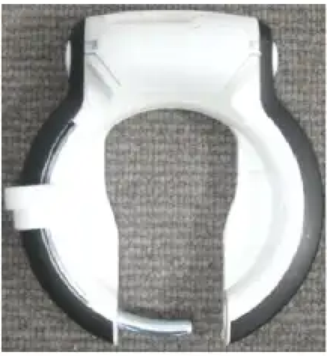


Figure 7. – Unsecured

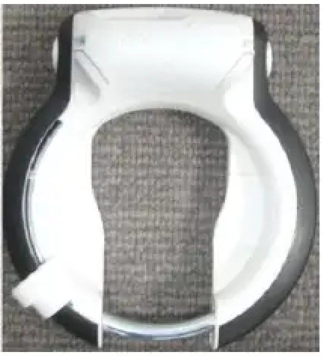


Figure 8. – Locked

Figure 7 presents the condition the leaver is in when the lock is Unlocked and the leaver is unsecured and is still able to move. This condition happens when the user Unlocks the lock and the spring inside the lock is not able to move the leaver completely in the Unlocked condition of Figure 6 due to an object (eq. spokes, hand) blocking this. This is an abnormal condition since the lock can now either be put in the Unlocked secured leaver condition from Figure 6 or in the Locked condition from Figure 8. The logic status output port will report Unlocked (LOW) in both the Unlocked secured (Fig 6) and Unlocked unsecured conditions (Fig 7), if the leaver is moved from the Unlocked unsecured into the Locked condition from Figure 8 the status output port will be updated and report Locked (HIGH).

This status update, the unexpected locking can happen anytime when the lock is in the Unlocked condition and the software designer should be aware of this condition and make sure their software is able to cope with status updates like this.

Microcontroller Mode – Power Up

The Power-Up sequence presented in Figure 9 is assuming power is applied through the power Vdd Pin 1 in microcontroller mode. In Power down the eRL logic inputs A and B shall be driven low and kept low during the complete initialization phase, status output will be undefined and floating in this situation. This setup will result in the lowest leakage current possible and will be in the order of less than 100nA.

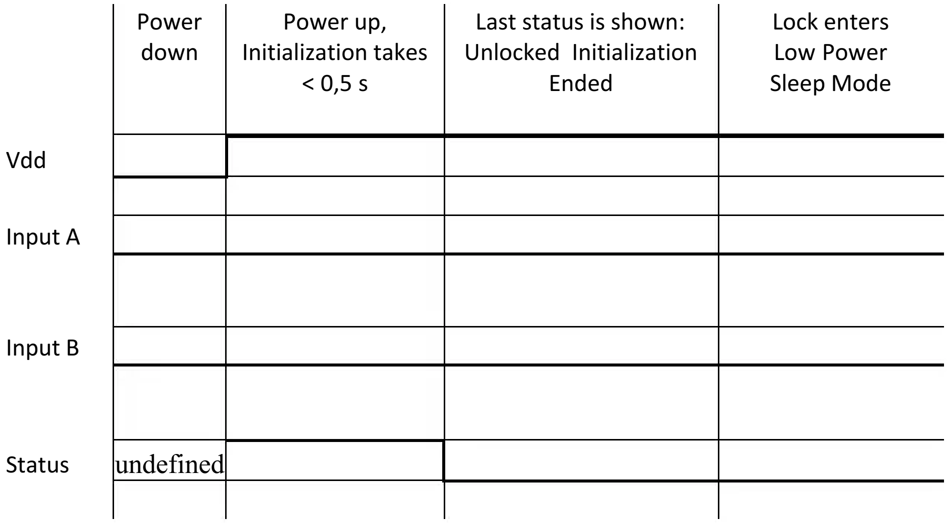

Power down
Power up, Initialization takes < 0,5 s
Last status is shown: Unlocked Initialization Ended
Lock enters Low Power Sleep Mode
Vdd
Input A
Input B
Status
undefined

Figure 9: Power-Up Sequence

After the completion of the initialization phase, which is initiated after power up and lasting 500ms the current lock status is provided through the status pin 5. By no means shall the status pin 5 be used to check for the completion of the initialization phase, you shall always wait 500ms before the status pin 5 can be checked after Power-Up.

Microcontroller Mode – Unlocking / Locking

The Unlocking / Locking sequence presented in Figure 10 and 11 is assuming power is applied continuously through the power Vdd Pin 1 in microcontroller mode. In Low Power Sleep Mode the eRL logic inputs A and B shall be driven low and kept low until you want to Unlock or Lock the eRL, status output will be defined and representing the current lock state. The Locking sequence from Figure 11 is assuming the bicycle-user moves the eRL leaver to lock the bicycle.

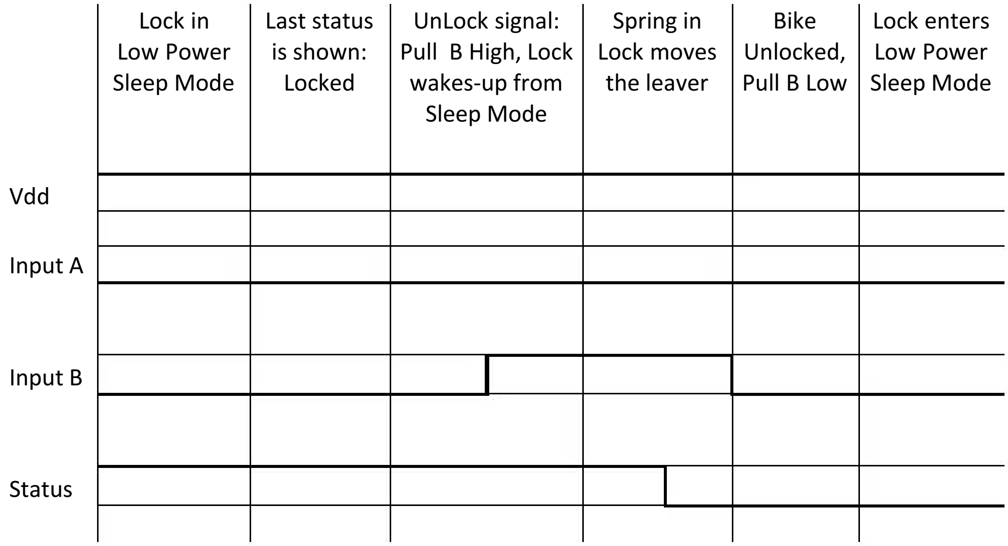

Lock in Low Power Sleep Mode
Last status is shown: Locked
UnLock signal: Pull B High, Lock wakes-up from Sleep Mode
Spring in Lock moves the leaver
Bike Unlocked, Pull B Low
Lock enters Low Power Sleep Mode
Vdd
Input A
Input B
Status

Figure 10: Unlocking Sequence

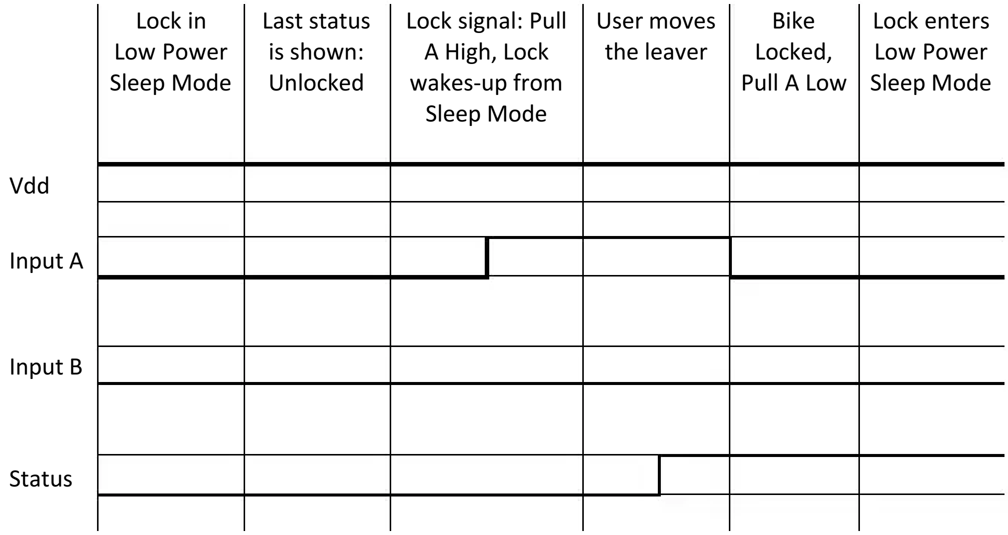

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
Lock signal: Pull A High, Lock wakes-up from Sleep Mode
User moves the leaver
Bike Locked, Pull A Low
Lock enters Low Power Sleep Mode
Vdd
Input A
Input B
Status

Figure 11: Completed Locking Sequence

If the bicycle-user does not complete the locking sequence by moving the eRL leaver the sequence to follow is represented in Figure 12, you shall use a timeout of minimum 18 seconds before logic control input A is put back into the low state. During those 18 seconds it is possible that the status changes from Unlocked into Locked as a result from the bicycle-user moving the leaver, therefor you should monitor the status pin 5 regularly for change during those 18 seconds. After an internal timeout of about 15 seconds the eRL moves automatically back into the save Unlocked position making it impossible to move the leaver by the bicycle-user.

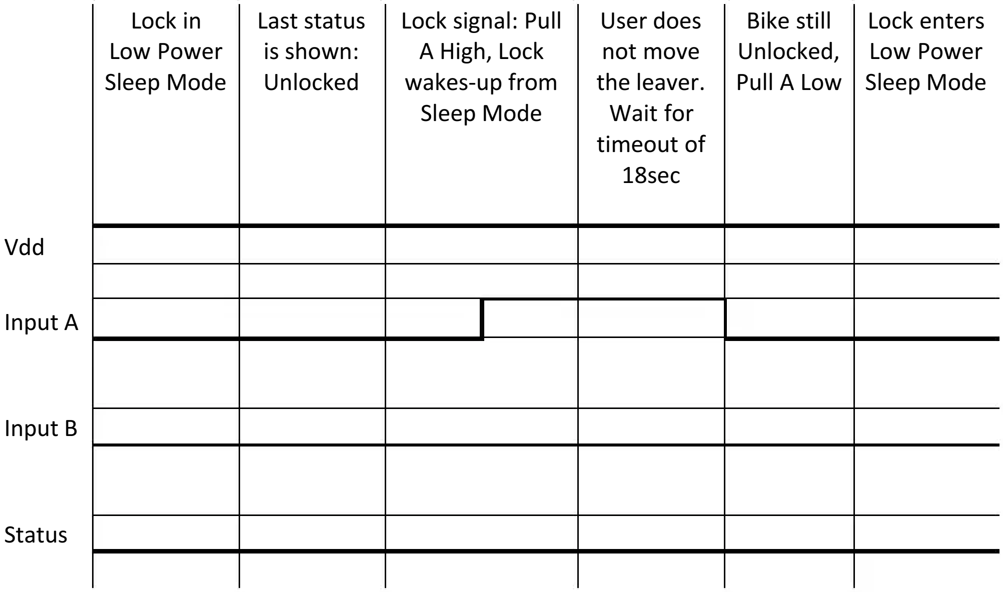

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
Lock signal: Pull A High, Lock wakes-up from Sleep Mode
User does not move the leaver. Wait for timeout of 18sec
Bike still Unlocked, Pull A Low
Lock enters Low Power Sleep Mode
Vdd
Input A
Input B
Status

Figure 12: Uncompleted Locking Sequence

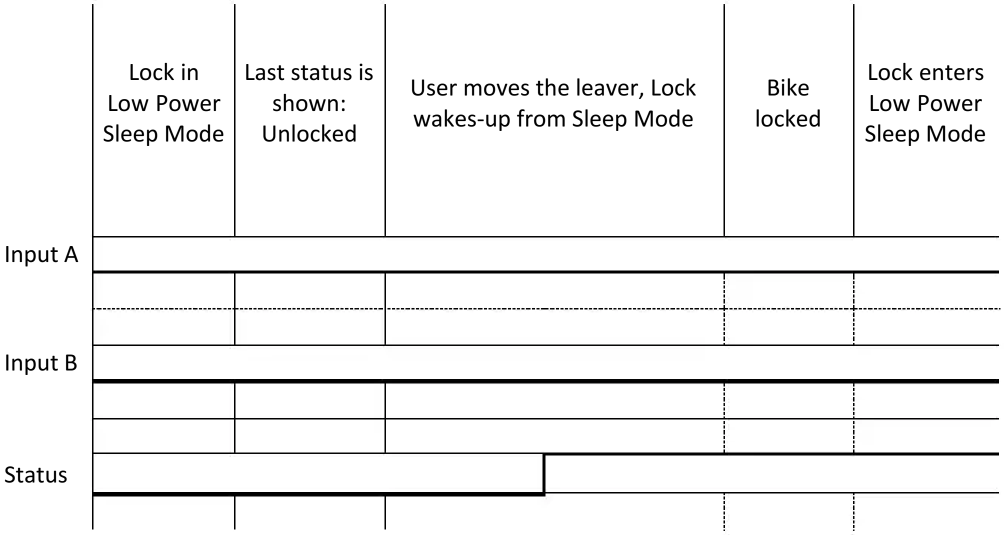

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
User moves the leaver, Lock wakes-up from Sleep Mode
Bike locked
Lock enters Low Power Sleep Mode
Input A
Input B
Status

Figure 13: Unexpected Locking Sequence

If the lock is Unlocked and the leaver is unsecured the bicycle-user can at any time move the leaver into the Locked condition and thereby locking the lock, this unexpected locking is represented in figure 13. This status will be updated and the software designer should be aware of this condition and make sure their software is able to cope with status updates like this.

H-Bridge Controlled Mode – Power Up

The Power-Up sequence presented in Figure 14 is assuming power is applied through the power Vdd Pin 1 similarly as in the microcontroller mode. In Power down both the eRL logic inputs A and B will be either floating or driven low depending on the type of H-Bridge used. This condition should be kept until the initialization phase is completed, status output will be undefined and floating in this situation. This setup will result in the lowest leakage current possible and will be in the order of less than 100nA.

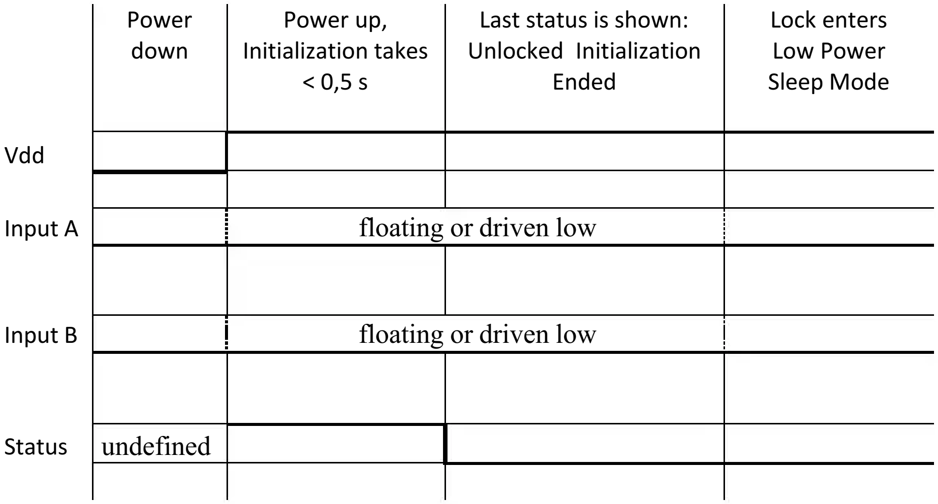

Power down
Power up, Initialization takes < 0,5 s
Last status is shown: Unlocked Initialization Ended
Lock enters Low Power Sleep Mode
Vdd
Input A
floating or driven low
Input B
floating or driven low
Status
undefined

Figure 14: Power-Up Sequence

After the completion of the initialization phase, which is initiated after power up and lasting 500ms the current lock status is provided through the status pin 5. By no means shall the status pin 5 be used to check for the completion of the initialization phase, you shall always wait 500ms before the status pin 5 will be checked after Power-Up. The logic inputs A and B shall both be floating or driven low at power up and kept in this state until completion of the initialization phase.

One note of caution is the switching speed in the H-Bridge controlled mode, when logic input A is pulled high by the H-Bride within 10ms logic input B shall be pulled low and vice versa.

H-Bridge Controlled Mode – Unlocking / Locking

The Unlocking / Locking sequence presented in Figure 15 and 16 is assuming power is applied continuously through the power Vdd Pin 1 similarly as in the microcontroller mode. In Low Power Sleep Mode the eRL logic inputs A and B shall both be floating or driven low until you want to Unlock or Lock the eRL, status output will be defined and representing the current lock state. The Locking sequence from Figure 16 is assuming the bicycle-user moves the eRL leaver to lock the bicycle.

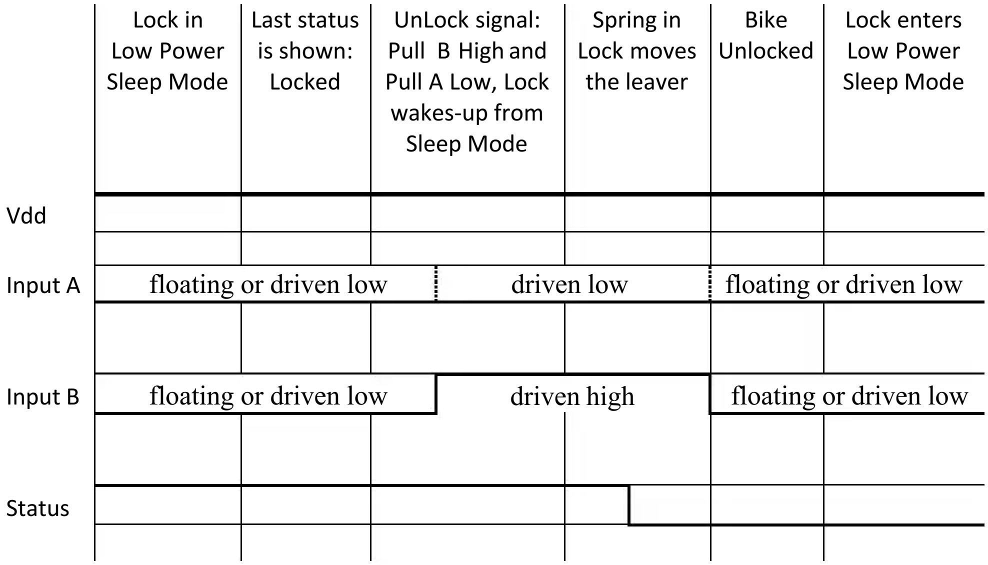

Lock in Low Power Sleep Mode
Last status is shown: Locked
UnLock signal: Pull B High and Pull A Low, Lock wakes-up from Sleep Mode
Spring in Lock moves the leaver
Bike Unlocked
Lock enters Low Power Sleep Mode
Vdd
Input A
floating or driven low
driven low
floating or driven low
Input B
floating or driven low
driven high
floating or driven low
Status

Figure 15: Unlocking Sequence

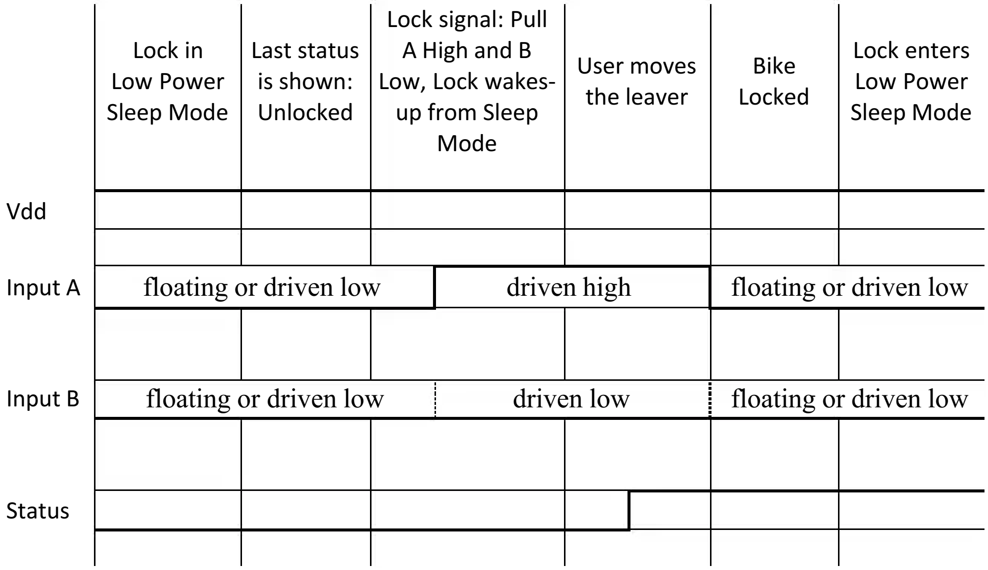


Figure 16: Completed Locking Sequence

If the bicycle-user does not complete the locking sequence by moving the eRL leaver the sequence to follow is represented in Figure 17. You shall use a timeout of minimum 18 seconds before logic control input A and B is moved into the floating or driven low state, before you can try to lock the eRL again. During those 18 seconds it is possible that the status changes from Unlocked into Locked as a result from the bicycle-user moving the leaver, therefor you should monitor the status pin 5 regularly for change during those 18 seconds. After an internal timeout of about 15 seconds the eRL moves automatically back into the save Unlocked position making it impossible to move the leaver by the bicycle-user.

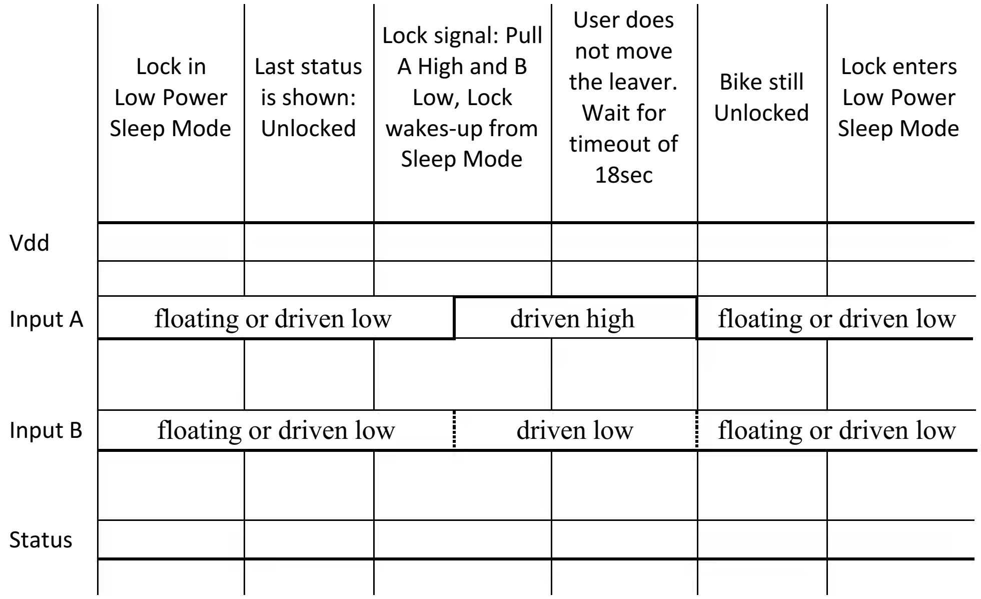

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
Lock signal: Pull A High and B Low, Lock wakes-up from Sleep Mode
User does not move the leaver. Wait for timeout of 18sec
Bike still Unlocked
Lock enters Low Power Sleep Mode
Vdd
Input A
floating or driven low
driven high
floating or driven low
Input B
floating or driven low
driven low
floating or driven low
Status

Figure 17: Uncompleted Locking Sequence

If the lock is Unlocked and the leaver is unsecured the bicycle-user can at any time move the leaver into the Locked condition and thereby locking the lock, this unexpected locking is represented in figure 18. This status will be updated and the software designer should be aware of this condition and make sure their software is able to cope with status updates like this.

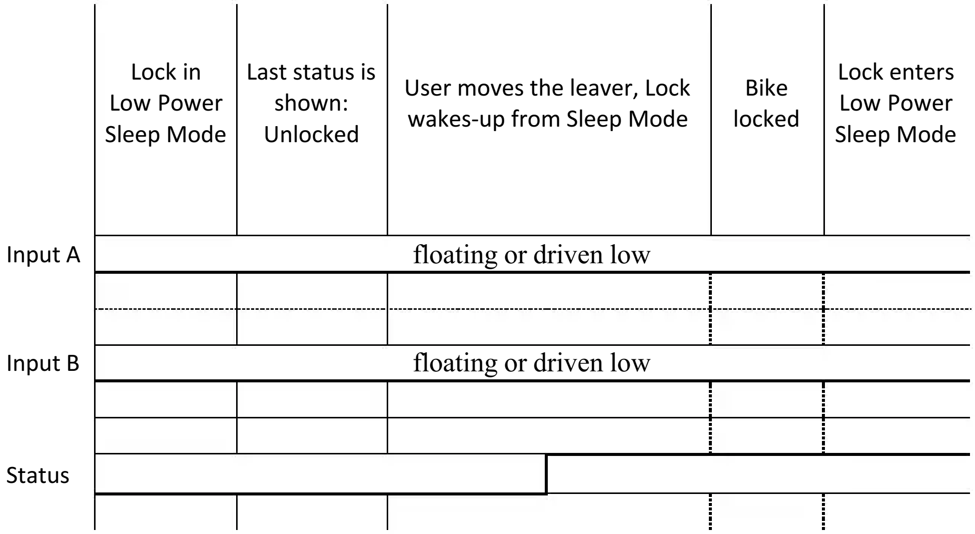
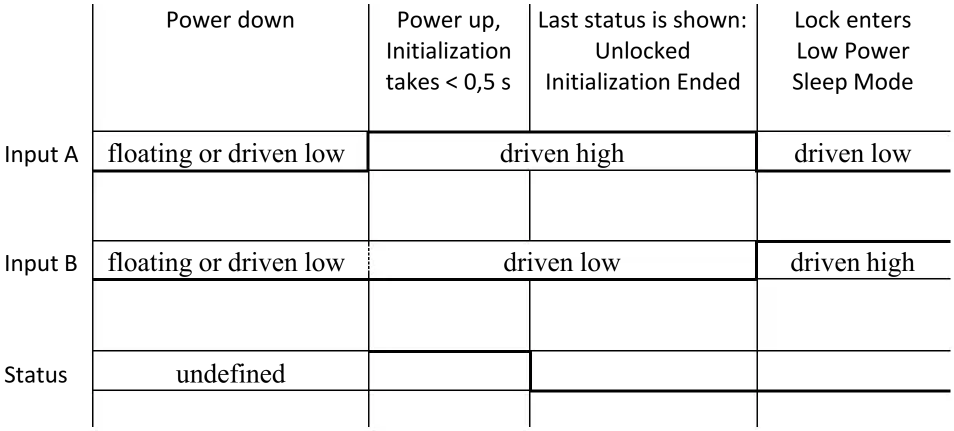

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
User moves the leaver, Lock wakes-up from Sleep Mode
Bike locked
Lock enters Low Power Sleep Mode
Input A
floating or driven low
Input B
floating or driven low
Status

Figure 18: Unexpected Locking Sequence

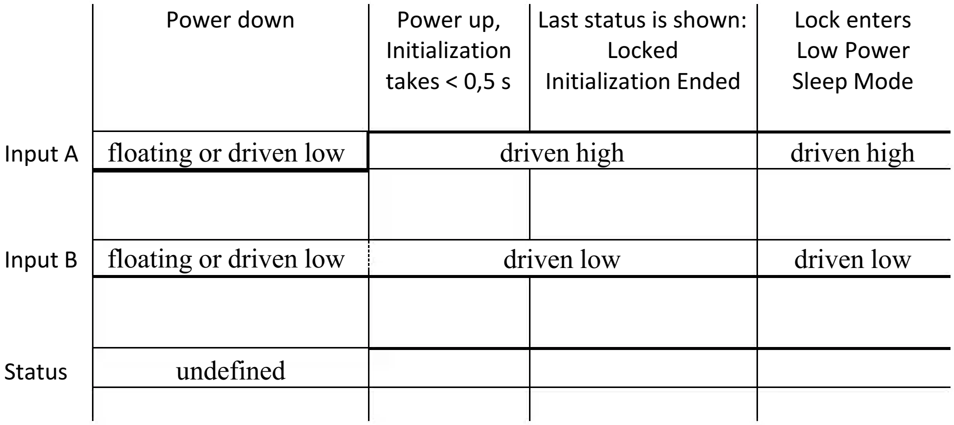
H-Bridge Powered Mode – Power Up

The Power-Up sequence presented in Figure 19a and 19b is assuming power is not applied through the normal power Vdd Pin 1 but through the H-Bridge configuration. When this mode is used power to the eRL is provided through either the logic inputs A or B. In Power down both the eRL logic inputs A and B will be either floating or driven low depending on the type of H-Bridge used. This setup will result in the lowest leakage current possible and will be in the order of less than 100nA.



	Power down	Power up, Initialization takes < 0,5 s	Last status is shown: Unlocked Initialization Ended	Lock enters Low Power Sleep Mode
Input A	floating or driven low	driven high		driven low
Input B	floating or driven low	driven low		driven high
Status	undefined			

Figure 19a: Power-Up Sequence – Unlocked



	Power down	Power up, Initialization takes < 0,5 s	Last status is shown: Locked Initialization Ended	Lock enters Low Power Sleep Mode
Input A	floating or driven low	driven high		driven high
Input B	floating or driven low	driven low		driven low
Status	undefined			

Figure 19b: Power-Up Sequence – Locked

Some restrictions apply when using an H-Bride powered eRL setup as described. One of the restrictions is the minimum voltage the eRL can operate on will increase, check the value specified in the Chapter 6 (Electrical Operating Conditions). The second restriction is the minimum switching speed, when logic input A is pulled high by the H-Bride virtually instantly (within 10µs) logic input B shall be pulled low and vice versa. This is needed otherwise the eRL will be without any power supply for a prolonged period, this can be overcome by mounting a large external capacitor from pin 1 to pin 3 to store energy for this event.

H-Bridge Powered Mode – Unlocking / Locking

The UnLocking / Locking sequence presented in Figure 20 and 21 is assuming power is not applied through the normal power Vdd Pin 1 but through the H-Bridge configuration. In Low Power Sleep Mode the eRL logic inputs A and B shall always be driven in the opposite state, status output will be defined and representing the current lock state. The Locking sequence from Figure 21 is assuming the bicycle-user moves the eRL leaver to lock the bicycle.

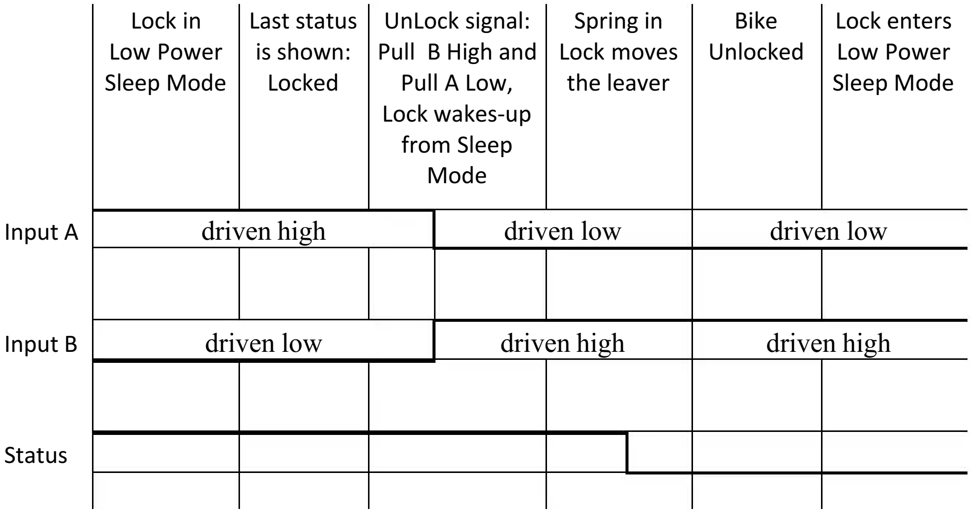

Lock in Low Power Sleep Mode
Last status is shown: Locked
UnLock signal: Pull B High and Pull A Low, Lock wakes-up from Sleep Mode
Spring in Lock moves the leaver
Bike Unlocked
Lock enters Low Power Sleep Mode
Input A
driven high
driven low
driven low
Input B
driven low
driven high
driven high
Status

Figure 20: Unlocking Sequence

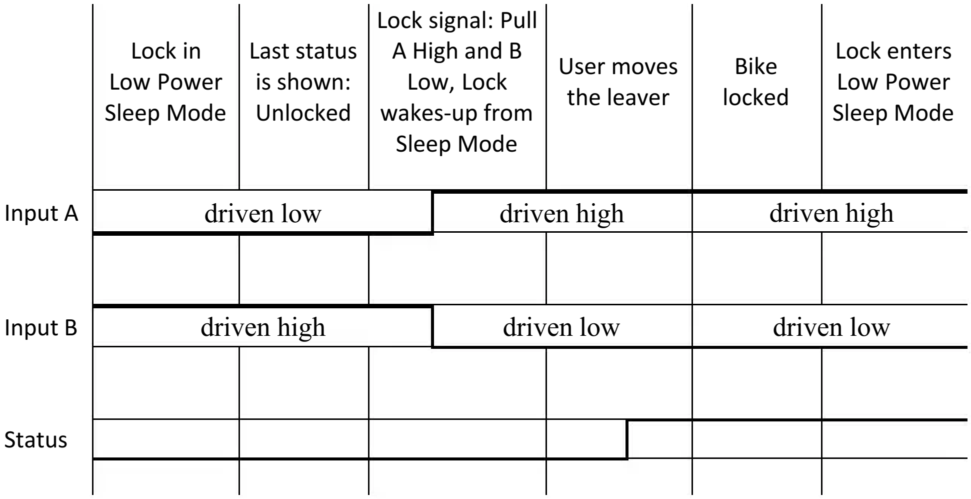

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
Lock signal: Pull A High and B Low, Lock wakes-up from Sleep Mode
User moves the leaver
Bike locked
Lock enters Low Power Sleep Mode
Input A
driven low
driven high
driven high
Input B
driven high
driven low
driven low
Status

Figure 21: Completed Locking Sequence

If the bicycle-user does not complete the locking sequence by moving the eRL leaver the sequence to follow is represented in Figure 22. You shall use a timeout of minimum 18 seconds before logic control A and B is driven in the opposite state, before you can try to lock the eRL again. During those 18 seconds it is possible that the status changes from unlocked into locked as a result of the bicycle-user moving the leaver, therefor you should monitor the status pin 5 regularly for change during those 18 seconds. After an internal timeout of about 15 seconds the eRL moves automatically back into the save Unlocked position making it impossible to move the leaver by the bicycle-user.

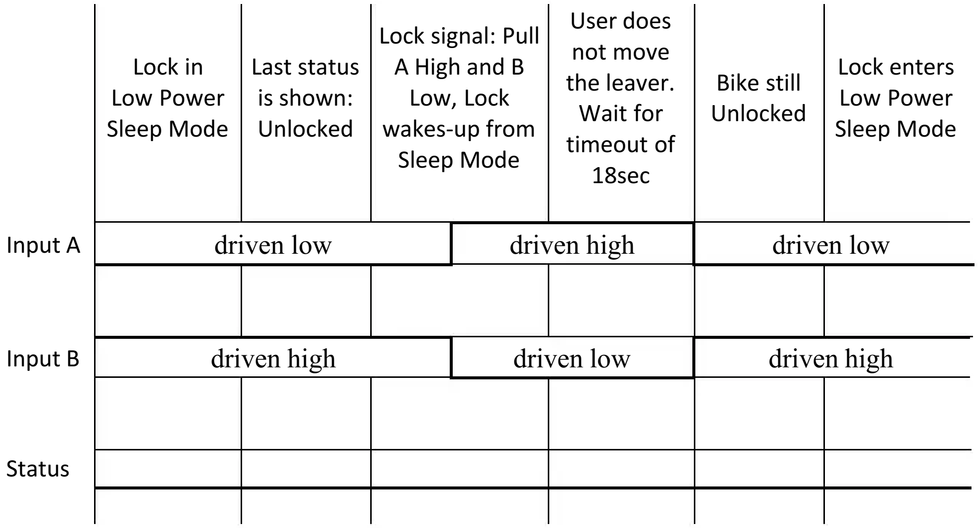

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
Lock signal: Pull A High and B Low, Lock wakes-up from Sleep Mode
User does not move the leaver. Wait for timeout of 18sec
Bike still Unlocked
Lock enters Low Power Sleep Mode
Input A
driven low
driven high
driven low
Input B
driven high
driven low
driven high
Status

Figure 22: Uncompleted Locking Sequence

If the lock is Unlocked and the leaver is unsecured the bicycle-user can at any time move the leaver into the Locked condition and thereby locking the lock, this unexpected locking is represented in figure 23. This status will be updated and the software designer should be aware of this condition and make sure their software is able to cope with status updates like this. The eRL logic inputs A and B shall be driven in the correct way after an unexpected locking event before any other command can be given.

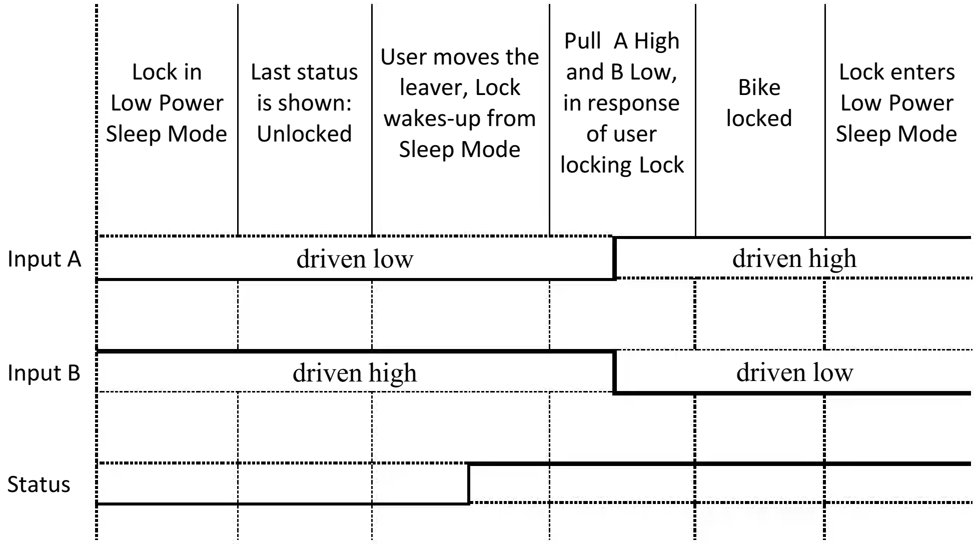

Lock in Low Power Sleep Mode
Last status is shown: Unlocked
User moves the leaver, Lock wakes-up from Sleep Mode
Pull A High and B Low, in response of user locking Lock
Bike locked
Lock enters Low Power Sleep Mode
Input A
driven low
driven high
Input B
driven high
driven low
Status

Figure 23: Unexpected Locking Sequence

4. Design considerations and recommendations

The current consumption of the eRL is volatile and unpredictable in nature due to the electric motor used. Peak currents can be as high as 500mA during stall conditions and low current situations of 1µA or smaller during sleeping conditions. Due to the nature of the rapid rising current consumption and volatile nature the power source of the eRL should be able to cope with these rapid varying conditions and situations. It is advised to over dimension the power source circuit and making sure it remains stable during rapidly changing load conditions.

It is recommended that the external pull-up resistor connected to the eRL status pin is configured in such a way that it can be switched off if the eRL status pin information is not needed. This can be done by using an internal pull-up resistor on the microcontroller I/O pin or an external conventional resistor of 100K that is powered from another I/O pin configured as output. The output I/O pin can be used in this case to switch the pull-up on or off by making the output respectively high or low. This will result in the lowest possible current consumption setup. It is advised to check periodically the status of the eRL status pin, an interval of 1 to 10 seconds will not increase the current consumption. Checking the eRL status pin is only needed if the lock is unlocked since it can change to the locked state at any moment in time.

If the microcontroller mode is being used to control the eRL it is advised to put some small resistors in the range of 1 upto 10K in series with the command input lines A and B. These resistors are only needed if long cables are being used to control the eRL, these long cables can pick-up static electricity which is able to harm your microcontroller I/O circuit.

In order to test the correct implementation of the eRL command protocol and response to the eRL status pin by the designer’s software and hardware implementation it is strongly advised to follow all and check the Test Scenarios explained in Chapter 5.

5. Test Scenarios

Test scenarios are test cases designed for the software designers that ensure that all possible situations and conditions are tested from end to end. The scenarios are independent tests; or a series of tests that follow each other, where each of them depends upon the output of the previous one. The scenarios were prepared by reviewing general functional requirements, and are designed to represent both typical and unusual situations that may occur in the user case. The test scenarios are executed through the use of test procedures given in Appendix A, the procedures define a series of steps necessary to perform one or more test scenarios.

6. Electrical Characteristics

Absolute Maximum Electrical Ratings[†]

Characteristic	
Ambient temperature under bias	-25°C to +85°C
Ambient temperature during operation	-20°C to +55°C
Supply Voltage Vdd pin with respect to Vss (Idle)	18V
Supply Voltage Vdd pin with respect to Vss (Running)	16V
Supply Voltage Vdd pin with respect to Vss (Stall)	10V
Supply Current Vdd pin	250mA
Peak (10s) Supply Current Vdd pin @ 10V (Stall)	500mA
All logic inputs and outputs	(Vss-0.3V) to (Vdd+0.3V)
Maximum current sunk by outputs	25mA
ESD protection on all pins (HBM; MM)	≥ 2kV; ≥ 400V

Standard Electrical Operating Conditions (unless otherwise stated)

Operating temperature -20°C ≤ TA ≤ +55°C

Characteristic	**Min**	**Typ.**	**Max**	**units**	**Conditions**
Supply Voltage (Vdd)	4.8	8	14	V	Microcontroller Mode
Supply Voltage (Vdd)	4.8	8	14	V	H-Bridge Controlled Mode
Supply Voltage (Vdd)	5.2	8	14	V	H-Bridge Powered Mode
Supply Current		90		mA	Motor Running
Peak Supply Current			350	mA	Motor Startup < 100ms
Motor Stall Current			500	mA	Motor Stall < 10s @ 8V
Power-saving Current[1]		1	7	µA	Vdd = 8V, (Sleep mode)
Control Input A / B	0		1.5	V	Logic level low
Control Input A / B	2.7		Vdd	V	Logic level high
Status Output Voltage	0		Vdd	V	External Pull-up
Status Sink Current			20	mA	Open drain output
Start-up Time		290	500	ms	Power up
Unlocking Time	1.5	1.8	2.1	s	Locked -> Unlocked
Locking Timeout	12	15	18	s	Unlocked -> Unlocked
Stall Timeout	7	10	15	s	Vdd = 8V
A / B debouncing time	17	20	23	ms	

1: Current is excluding any additional current from external pull-ups.

Appendix A – Test scenarios

Test Case Title	**Current Status**	**Description**	**Expected Status**	**Muralis Comments**	**Test Completed**
	Unlocked/Locked Status Pin		Unlocked/Locked Status Pin		Failed / Passed Check
Power-Up Sequence	Unlocked	Don't give any command and wait for 20 seconds.	Unlocked	The Lock shall remain idle.	
Uncompleted Locking Sequence	Unlocked	Give a Locking command and don't move the leaver, wait for 20 seconds timeout.	Unlocked	The Lock shall return to unlock secured after timeout. Making it impossible to move the leaver again	
Interrupted Locking Sequence	Unlocked	Give a Locking command, move the leaver halfway and wait for 20 seconds.	Unlocked	The Lock shall return to unlock secured after timeout. Making it impossible to move the leaver again	
Completed Locking Sequence	Unlocked	Give a Locking command and move the leaver to Locked position.	Locked	The Lock shall Lock successfully.	
Uncompleted Unlocking Sequence	Locked	Give an Unlocking command, block the leaver from opening into the Unlocked secured position.	Locked	The Lock shall put itself into the Locked condition again. Status always remained Locked during the test.	
Blocked Unlocking Sequence	Locked	Give an Unlocking command, block the leaver halfway from opening completely and move the leaver after sometime into the Locked position again.	Locked	Status will be "Unlocked" when lock is halfway and updated again when Lock is put into Locked position.	
Completed Unlocking Sequence	Locked	Give an Unlocking command.	Unlocked	Spring inside the Lock shall pull the leaver into the Unlocked secured position.	